UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,978	03/17/2004	Raymond Chow	VP111	3914

20178 7590 09/04/2008

EPSON RESEARCH AND DEVELOPMENT INC
INTELLECTUAL PROPERTY DEPT
2580 ORCHARD PARKWAY, SUITE 225
SAN JOSE, CA 95131

EXAMINER	
GUERTIN, AARON M	

ART UNIT	PAPER NUMBER
2628	

MAIL DATE	DELIVERY MODE
09/04/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,978	CHOW ET AL.	
	Examiner	Art Unit	
	AARON M. GUERTIN	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,18-20 and 22-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,18-20 and 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

- Claims 1-6, 18-20, and 22-25 are presented for examination.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Publication No.: US 2002/0130870 A1 (Ebihara) in view of U.S. Patent No. 4,446,459 (Bond).

3. Regarding claim 1, Ebihara teaches of a method for increasing the processing capability of a device ([0054] - *the user can create contents to fully exhibit the functionality of the graphics processor 2 and increase the performance of the graphics processor 2. The user can also tune his or her image processing program easily. The present invention offers significant benefits and excellent support for creating graphics-related contents or an image processing program expected to put a large load on a computer, such as 3D image processing…*), comprising: **requesting by a processor access to a module in a display controller** (control processor 1 implements an access by resetting a processing clock and switches the dependency of processing to

processor 2 which is activated by the clock that has been set by processor 1; these steps are conducted in display controller of figure 5 (containing GSBs 100); [0051] - *In response to the draw ready signal supplied from the control processor 1, the time counter 3 resets the time count value and begins measurement of a processing time for each frame. The graphics processor 2 changes the buffers in response to the reception of the draw ready signal. The graphics processor 2 provides the image in the buffer B on the display device and generates a frame image through image processing such as geometry processing. The graphics processor 2 draws the resulting frame image into the buffer A. After completion of loading of the frame image into the buffer A, the graphics processor 2 supplies the draw complete signal to the control processor 1…*); **processing continuously in the processor until notification that the module in the display controller is available** (Processor 2 continues to process until the frame is complete and then issues the draw complete, indicating the module is available; Fig. 3 shows wherein the processing is continuous until the end count signal, or draw complete signal has been sent; and [0051] - *After completion of loading of the frame image into the buffer A, the graphics processor 2 supplies the draw complete signal to the control processor 1. As shown in FIG. 3, the draw complete signal goes "HIGH" for one clock period to indicate that the signal is produced from the graphics processor 2. The time counter 3 terminates the measurement of the time when it determines the output of the draw complete signal. The time count value thus obtained indicates the time interval during which the graphics processor 2 performs the image processing, that is, the state of the execution load.*). Ebihara teaches the limitations of claim 1 above,

however Ebihara fails to specifically teach **sending by a multiplexer in the display controller an available signal to a pin in the processor, the pin in the processor having a dual function, wherein one of the dual functions is to notify the processor that the module is available and accessing by the processor the module in the display controller after sending the first available signal via the pin**.

Bond is analogous art and further teaches of **sending by a multiplexer in the display controller an available signal to a pin in the processor, the pin in the processor having a dual function** (dual function is wherein the state of the system is busy or not busy, which is supplied by multiplexer k11; and [Column 4, lines 64-68] – *Referring now to FIG. 4, NAND gate M12 receives Signal ADDS 140 (Address 14) at pin 13 from the system of FIG. 2, and receives Signal BSY0 (Busy) at pin 12 from pin K6-6 as discussed, below…* and [Column 6, lines 17-40] - *The "Busy" system accomplishing this handshaking includes "Busy" flipflop K6, tristate multiplexer K11, two pulse generators receiving signals from multiplexer K11, and AND/OR device K9.*), **wherein one of the dual functions is to notify the processor that the module is available and accessing by the processor the module in the display controller after sending the first available signal via the pin** (the incorporation of the rational above, and also the [Abstract] - *For transmission of data from the computer to the peripheral, the computer initially clears a flipflop which provides a select signal to a multiplexer. When the computer is ready to provide data to the peripheral, it produces a data available signal or data strobe signal while the data is being provided to the interface*).

All the elements of claim 1 are known in Ebihara in view of Bond, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Ebihara the implementation of an available signal engaged by a multiplexer for a pin that provides the processor of the status of the module as suggested by Bond, as doing so would provide the means for a display controller that incorporates the use of signals that are active only upon the status changes within a system to eliminate the need for continuous polling of the devices and rely upon an indication sent once a process has been completed.

4. Regarding claim 2, Ebihara and Bond teach the limitations of claim 1, the rationale disclosed in the rejection incorporated herein, and Ebihara further teaches of **wherein requesting by a processor access to a module in a display controller includes transmitting an access request signal to the module in the display controller** (the access signal stems from a draw ready signal. The draw ready signal as in fig. 3 begins to count and processing of data; processing of processor 2 is continuous until the draw complete signal which is sent by processor 2 upon the completion the frame data; [0042] - *More specifically, the graphics processor 2 carries out geometry processing (coordinate conversion) and rendering (drawing) to load a frame image into an off-screen buffer, such as buffer A, in response to a draw ready signal (process enable signal) from the control processor 1.*).

5. Regarding claim 3, Ebihara and Bond teach the limitations of claim 1 above, the rejection disclosed in the rejection incorporated herein, and Ebihara further teaches of **wherein processing continuously until notification by the module in the display controller includes an available signal** ([Fig. 3] shows that processing in Buffer A is continuous until the end count and the draw complete signal goes High; [0051] - *After completion of loading of the frame image into the buffer A, the graphics processor 2 supplies the draw complete signal to the control processor 1. As shown in FIG. 3, the draw complete signal goes "HIGH" for one clock period to indicate that the signal is produced from the graphics processor 2. The time counter 3 terminates the measurement of the time when it determines the output of the draw complete signal. The time count value thus obtained indicates the time interval during which the graphics processor 2 performs the image processing, that is, the state of the execution load.*). Bond further teaches of a **display controller including checking the pin in response to the available signal** ([Abstract] - *For transmission of data from the computer to the peripheral, the computer initially clears a flipflop which provides a select signal to a multiplexer. When the computer is ready to provide data to the peripheral, it produces a data available signal or data strobe signal while the data is being provided to the interface…* [Column 4, lines 64-68] – *Referring now to FIG. 4, NAND gate M12 receives Signal ADDS 140 (Address 14) at pin 13 from the system of FIG. 2, and receives Signal BSY0 (Busy) at pin 12 from pin K6-6 as discussed, below…* and [Column 6, lines 17-40] - *The "Busy" system accomplishing this handshaking includes "Busy" flipflop K6,*

tristate multiplexer K11, two pulse generators receiving signals from multiplexer K11, and AND/OR device K9.).

6. Regarding claim 4, Ebihara and Bond teach the limitations of claim 1 above, the rejection disclosed in the rejection incorporated herein, and Bond further of wherein sending an available signal further includes: **sending a non-available signal to the pin in the processor while the module is not available** ([Column 10, lines 31-47] - *A logical `1` in any bit position can be a true state (i.e., an `01` byte indicates a Device Unavailable condition…The present embodiment requires a command byte to set up for conversing with a display generator… enabling interrupts, and both hard and soft initialization of the display generators.*)**; wherein the multiplexer in the display controller selects either a wait signal or a busy signal to send to the pin in the processor; wherein the multiplexer in the display controller sends the available signal to the pin when the multiplexer is selecting the busy signal and the busy signal indicates that the module is available** ([Column 6, lines 17-40] - *T(10) As shown in FIG. 4, the present invention provides handshaking for data transfers between the computer and any display generator. For transmission of data from the present interface to a display generator, the interface provides an active signal ODR (output data ready), to that display generator when the data to be transmitted is on the interface's output lines and is ready for transmission. In response, the display generator strobes in or receives the data, and provides to the interface a Signal ODA (output data acknowledge) pulse to return signal ODR to its normal, "inactive" state. For*

transmission of data from a display generator to the present interface and thence to the computer, that display generator provides signal IDR (input data ready) to the interface. In response, the present invention provides signal IDA (input data acknowledge) to cause signal IDR to return to its normal state. The "Busy" system accomplishing this handshaking includes "Busy" flipflop K6, tristate multiplexer K11, two pulse generators receiving signals from multiplexer K11, and AND/OR device K9.).

7. Regarding claim 5, Ebihara and Bond teach the limitations of claim 1 above, the rejection disclosed in the rejection incorporated herein, and Ebihara further discloses of **wherein accessing by the processor the module in the display further includes halting other processing by the processor and proceeding with the access to the module** (other processing is halted during the wait signal [Fig. 3] and [0053] - *In the above-mentioned embodiment, the draw ready signal and the draw complete signal are used to indicate the start and end timings of the time measurement. However, only the draw complete signal may be used for this same purpose. More specifically, the draw complete signal may be in a "HIGH" state (first enable signal) for the time period when the image processing is being performed and may be in a "LOW" state (second enable signal) for the time period when no image processing is being performed, as shown in FIG. 4. The time counter 3 uses the draw complete signal as the enable signal to allow the measurement of the time when the draw complete signal is in the "HIGH" state. The draw complete signal is in the "HIGH" state during operation and goes to "LOW" at the*

time of completion of the operation. The time counter 3 is enabled for the measurement of the time only during the operation of the graphics processor 2).

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Publication No.: US 2002/0130870 A1 (Ebihara) and U.S. Patent No. 4,446,459 (Bond) in view of U.S. Patent No. 5,287,471 (Katayose).

9. Regarding claim 6, Ebihara and Bond teach the limitations of claim 1 above, the rejection disclosed in the rejection incorporated herein. However, both Ebihara and Bond fail to specifically teach of **wherein requesting access to a module in a display controller further includes providing indirect addressing for communication**.

Katayose is analogous art and further teaches of a data transfer controller that operates to assist processing operations for a display controller and further wherein indirect addressing is used when transferring the content from the memory to the display ([Column 5, lines 56-61] - *the content of RP 103 indicates the leading address of the transfer designation area 500. By an indirect addressing using the content of RP 103, CPU 11 can obtain the DMA-transferred data from the memory 2 (412)*.).

All the elements of claim 6 are known in Ebihara and Bond in view of Katayose, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Ebihara and Bond the implementation of indirect addressing as suggested by Katayose, as doing so would provide the means of having the ease of implementation of pointers, and ease of calling subroutines which would not have otherwise been addressable, with the indirect addressing feature provided by Katayose, for the display controller and having the advanced methods of being able to continuously process data though a controller might not be ready to receive the data and then to transport the data upon availability.

10. Claims 18-20, 22, and 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,028,733 (Ulicki) in view of U.S. Patent No. 4,446,459 (Bond) and in further view of U.S. Patent No. 6,930,730 (Maxon).

11. Regarding claim 18, Ulicki teaches of a display controller configured to receive a module request signal ([Abstract] - *A system for retrievably providing a video display of a pictorial information message on a video display device from video information stored, such as on a video tape, in a plurality of frames, unique pictorial information being stored in each frame for display thereof in response to a request therefor, the frames each including a plurality of segments with one displayable pictorial information…*), comprising: **a plurality of first modules connected to the controller** (the controller is

being considered as [Fig. 6, (44)] and the components are exemplary as [Fig. 6, (112, 114, 116, 154, etc…) and [Column 13, lines 55-68] thru [Column 14, lines 1-10] - *The control unit 110 decides which request it wants to process at a particular time utilizing conventional control logic in accordance with predetermined conditional relationships to be described in greater detail hereinafter. Once control unit 110 has established that it will service a particular tape number it switches that tape's audio and video signals into the data retrieval network by a control command to the audio and video multiplexers 112 and 114, respectively, which are conventional.*)**; a combinatorial multiplexer that selects one of the modules in the plurality of modules** ([Fig. 1, (46)] multiplexer 46 selects from the bank of tapes 42 in figure 1); **an input/output (I/O) multiplexer selecting a signal received from the combinatorial multiplexer** (tape controller 44 includes multiplexer 112 which receives the signal from the tape decks via mux 46;); **and a connector transmitting the output of the I/O multiplexer to a pin in a processor** (Figure 6 shows that the i/o multiplexer sends includes a connector 130 that transmits data to a frame select 126 wherein it is received by an input pin (processes which frames to be displayed) [Fig. 6, (130)])**.**

Ulicki teaches the limitations of claim 18 above, however Ulicki fails to specifically teach of **a wait signal or a busy, indicating whether the selected module is available; a pin in the processor having a dual function, wherein one of the dual functions is to notify the processor that the module is available.**

Bond is analogous art and further teaches of **a wait signal or a busy, indicating whether the selected module is available; a pin in the processor having a dual**

function, wherein one of the dual functions is to notify the processor that the module is available ([Column 6, lines 17-40] - *T(10) As shown in FIG. 4, the present invention provides handshaking for data transfers between the computer and any display generator. For transmission of data from the present interface to a display generator, the interface provides an active signal ODR (output data ready), to that display generator when the data to be transmitted is on the interface's output lines and is ready for transmission. In response, the display generator strobes in or receives the data, and provides to the interface a Signal ODA (output data acknowledge) pulse to return signal ODR to its normal, "inactive" state. For transmission of data from a display generator to the present interface and thence to the computer, that display generator provides signal IDR (input data ready) to the interface. In response, the present invention provides signal IDA (input data acknowledge) to cause signal IDR to return to its normal state. The "Busy" system accomplishing this handshaking includes "Busy" flipflop K6, tristate multiplexer K11, two pulse generators receiving signals from multiplexer K11, and AND/OR device K9.*).

.All the elements of claim 18 are known in Ulicki in view of Bond, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Ulicki the implementation of an available signals engaged by a multiplexer for a pin that provides the processor of the status of the module as suggested by Bond, as doing so would provide the means for a display controller that incorporates the use of signals that are active only upon the status changes within a

system to eliminate the need for continuous polling of the devices and rely upon an indication sent once a process has been completed.

Ulicki and Bond teach all of the limitations of claim 18 above, however Ulicki and Bond both fail to teach wherein the **modules are internal to the controller**.

Maxon is analogous art that further teaches of **modules are internal to the controller** ([Claim 15]).

All the elements of claim 18 are known in Ulicki and Bond in view of Maxon, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Ulicki and Bond the implementation of internalizing the AV modules to the controller as suggested by Maxon, as doing so would provide the means for an integrated system that increases control, accessibility, and speed.

12. Regarding claim 19, the rationale disclosed in the rejection of claim 18 is incorporated herein.

13. Regarding claim 20, Ulicki, Bond, and Maxon teach the limitations of claim 18 above, the rejection disclosed in the rejection incorporated herein, and Bond further teaches **wherein the module request signal is either a read or a write access request for one of the modules in the plurality of modules** (The read signal taught by Bond would activate the mans for a module to receive data; [Column 4, lines 64-68] thru [Column 5, lines 1-20] - *Referring now to FIG. 4, NAND gate M12 receives Signal*

ADDS 140 (Address 14) at pin 13 from the system of FIG. 2, and receives Signal BSY0 (Busy) at pin 12 from pin K6-6 as discussed, below. If either signal goes low (active), pin M12-11 produces a high signal which is provided to pin L15-4 …. if the display does not indicate that it is ready to receive data, as by producing a READ signal (which turns off ADDS 140), then the countdown continues for 256 milliseconds until the counters reach all zeros.).

14. Regarding claim 22, Ulicki, Bond, and Maxon teach the limitations of claim 18 above, the rejection disclosed in the rejection incorporated herein, and Ulicki further teaches **wherein a module request signal is sent by a processor** ([Fig. 6, (110)]) **to the display controller** ([Fig. 6, (44)]) **to request access to a requested module in the plurality of modules** ([Column 13, lines 55-68] thru [Column 14, lines 1-10] - *The control unit 110 decides which request it wants to process at a particular time utilizing conventional control logic in accordance with predetermined conditional relationships to be described in greater detail hereinafter. Once control unit 110 has established that it will service a particular tape number it switches that tape's audio and video signals into the data retrieval network by a control command to the audio and video multiplexers 112 and 114, respectively, which are conventional.*) and exemplary modules [Fig. 6, (112, 114, 116, 154, etc…), and Bond further teaches of **wherein the busy signal indicates whether the requested module is available** ([Column 6, lines 17-40] - *T(10) As shown in FIG. 4, the present invention provides handshaking for data transfers between the computer and any display generator. For transmission of data from the*

present interface to a display generator, the interface provides an active signal ODR (output data ready), to that display generator when the data to be transmitted is on the interface's output lines and is ready for transmission. In response, the display generator strobes in or receives the data, and provides to the interface a Signal ODA (output data acknowledge) pulse to return signal ODR to its normal, "inactive" state. For transmission of data from a display generator to the present interface and thence to the computer, that display generator provides signal IDR (input data ready) to the interface. In response, the present invention provides signal IDA (input data acknowledge) to cause signal IDR to return to its normal state. The "Busy" system accomplishing this handshaking includes "Busy" flipflop K6, tristate multiplexer K11, two pulse generators receiving signals from multiplexer K11, and AND/OR device K9.).

15. Regarding claim 23, the rationale disclosed within the rejection of claim 18 is incorporated herein.

16. Claims 18-20, 22, and 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,028,733 (Ulicki) and U.S. Patent No. 4,446,459 (Bond) in view of U.S. 6,930,730 (Maxon).

17. Regarding claim 24, Ulicki, Bond, and Maxon teach the limitations of claim 18, 22, and 23 above, the rejections disclosed in the rejections incorporated herein, and Ulicki teaches further of a **display controller** ([Fig. 6, (44)]) and Bond includes **checking a pin in response to the available signal** ([Abstract] - *For transmission of data from the computer to the peripheral, the computer initially clears a flipflop which provides a select signal to a multiplexer. When the computer is ready to provide data to the peripheral, it produces a data available signal or data strobe signal while the data is being provided to the interface…* [Column 4, lines 64-68] – *Referring now to FIG. 4, NAND gate M12 receives Signal ADDS 140 (Address 14) at pin 13 from the system of FIG. 2, and receives Signal BSY0 (Busy) at pin 12 from pin K6-6 as discussed, below…* and [Column 6, lines 17-40] - *The "Busy" system accomplishing this handshaking includes "Busy" flipflop K6, tristate multiplexer K11, two pulse generators receiving signals from multiplexer K11, and AND/OR device K9.*).

Ulicki, Bond, and Maxon teach the limitations of claim 24 above, however both Ulicki, Bond, and Maxon all fail to specifically teach of **wherein processing continuously until notification by the module in the display controller includes an available signal.**

Ebihara is analogous art and further teaches of **wherein processing continuously until notification by the module in the display controller includes an available signal** ([Fig. 3] shows that processing in Buffer A is continuous until the end count and the draw complete signal goes High; [0051] - *After completion of loading of the frame image into the buffer A, the graphics processor 2 supplies the draw complete*

signal to the control processor 1. As shown in FIG. 3, the draw complete signal goes "HIGH" for one clock period to indicate that the signal is produced from the graphics processor 2. The time counter 3 terminates the measurement of the time when it determines the output of the draw complete signal. The time count value thus obtained indicates the time interval during which the graphics processor 2 performs the image processing, that is, the state of the execution load.).

All the elements of claim 24 are known in Ulicki, Bond, and Maxon in view of Ebihara, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Ulicki, Bond, and Maxon the implementation of continuous processing until a notification of an available signal as suggested by Bond, as doing so would provide the means for a display controller that incorporates the use of signals that are active only upon the status changes within a system to eliminate the need for continuous polling of the devices and rely upon an indication sent once a process has been completed and therefore processing will not stall but continue which increases productivity.

18. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,028,733 (Ulicki), U.S. Patent No. 4,446,459 (Bond), and U.S. Patent No. 6,963,730 (Maxon), and in view of U.S. Patent No. 5,287,471 (Katayose).

19. Regarding claim 25, Ulicki, Bond, and Maxon teach the limitations of claims 18 and 22 above, the rejection disclosed in the rejection incorporated herein. However, Ulicki, Bond, and Maxon all fail to specifically teach of **wherein the processor communicates via indirect addressing**.

Katayose is analogous art and further teaches of a data transfer controller that operates to assist processing operations for a display controller and further wherein indirect addressing is used when transferring the content from the memory to the display ([Column 5, lines 56-61] - *the content of RP 103 indicates the leading address of the transfer designation area 500. By an indirect addressing using the content of RP 103, CPU 11 can obtain the DMA-transferred data from the memory 2 (412)*.).

All the elements of claim 6 are known in Ulicki, Bond, and Maxon in view of Katayose, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Ulicki, Bond, and Maxon the implementation of indirect addressing as suggested by Katayose, as doing so would provide the means of having the ease of implementation of pointers, and ease of calling subroutines which would not have otherwise been addressable, with the indirect addressing feature provided by

Katayose, for the display controller and having the advanced methods of being able to continuously process data though a controller might not be ready to receive the data and then to transport the data upon availability.

Response to Arguments

20. Applicant's arguments with respect to claims 1-6, 18-20, and 22-25 have been considered but are moot in view of the new ground(s) of rejection.

21. Applicant is respectfully advised that previous art from prior office actions is being considered related art.

Conclusion

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AARON M. GUERTIN whose telephone number is (571)270-1547. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aaron M. Guertin
Examiner, Art Unit 2628
August 17, 2008
/AMG/

/XIAO M. WU/
Supervisory Patent Examiner, Art Unit 2628